ABSTRACT

A method is provided for manufacturing a multi-layer wiring circuit substrate. A first metal layer is selectively etched in first areas to reduce a thickness of the metal layer in the first areas and to form protrusions in other areas which extend above the etched areas. An interlayer-insulating layer is formed to overlie the etched areas of the first metal layer. The interlayer-insulating layer has an inner surface which confronts the etched first areas and an outer surface remote from the inner surface, such that the protrusions extend through the interlayer-insulating layer and have ends exposed at the outer surface. A second metal layer is then provided in conductive communication with the exposed ends of the protrusions, and the first and second metal layers are selectively patterned from surfaces remote from the interlayer-insulating layer.